

source and destination register operands with all of the scoreboard entries. If a match is found, the scoreboard 600 provides a hardware interlock between any unfinished load or long latency operation and a younger instruction that has data/output dependency with the unfinished load or long latency operation. In such case, the younger instruction is stalled in the D stage 314 until the unfinished load or long latency instruction's scoreboard entry is invalidated. The younger instruction is stalled until a terminating event occurs in relation to the unfinished load or long latency operation. For a load operation, the terminating event is the return of the load data from the data cache or from memory. For a long latency operation, the terminating event that triggers invalidation of that instruction's scoreboard entry occurs when the long latency operation enters the A4, or T, stage 360 without being bumped.

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Amal.

#### REMARKS

For this preliminary amendment, the specification is being amended to correct minor typographical errors. No new matter is being added.

The application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 794-3600.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Box Non-Fee Amendment, Commissioner for Patents, Washington, D.C. 20231, on May 8, 2001.

Shireen Irani Bacon 5/8/01  
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Respectfully submitted,

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## APPENDIX B

The Preliminary Amendment amends the Specification to read as follows:

On page 8, lines 8-23:

Also during the D stage 314, the scoreboard 600 (FIGURE 6) is read and updated. The scoreboard 600 is a structure with information concerning unfinished loads and long latency instructions. An unfinished load instruction is an instruction whose scoreboard entry is valid but that has not yet returned its load data. All instructions access the scoreboard 600 in the D Stage 314 in order to check for dependencies. When a new instruction enters the D stage 314, it compares its source and destination register operands with all of the scoreboard entries. If a match is found, the scoreboard 600 provides a hardware interlock between any unfinished load or long latency operation and a younger instruction that has data/output dependency with the unfinished load or long latency operation. In such case, the younger instruction is stalled in the D stage 314 until the unfinished load or long latency instruction's scoreboard entry is invalidated. The younger instruction is stalled until a terminating event occurs in relation to the unfinished load or long latency operation. For a load operation, the terminating event is the return of the load data from the data cache or from memory. For a long latency operation, the terminating event that triggers invalidation of that instruction's scoreboard entry occurs when the long latency operation enters the A4, or T, stage 360 without being bumped. [Sharada: what does "bumped" mean?]

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